SEMICONDUCTOR MULTI-PACKAGE MODULE HAVING WIRE BOND INTERCONNECTION BETWEEN STACKED PACKAGES AND HAVING ELECTRICAL SHIELD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/411,590, filed 17 September 2002, which is hereby incorporated herein by reference.

[0002] This application is related to ~~U.S. Application No. (Atty~~ Docket No. CPAC.1017-2), titled "Semiconductor multi-package module having wire bond interconnection between stacked packages"; ~~U.S. Application No. (Atty Docket No.~~ CPAC.1017-3), titled "Semiconductor multi-package module having package stacked over ball grid array package and having wire bond interconnection between stacked packages"; ~~U.S. Application No. (Atty~~ Docket No. CPAC.1017-5), titled "Semiconductor multi-package module having package stacked over die-up flip chip ball grid array package and having wire bond interconnect between stacked packages"; ~~U.S. Application No. (Atty Docket~~ No. CPAC.1017-6), titled "Semiconductor multi-package module having package stacked over die-down flip chip ball grid array package and having wire bond interconnect between stacked packages"; U.S. Application No. ~~(Atty Docket No. CPAC.1017-7~~), titled "Semiconductor multi-package module including stacked-die packages and having wire bond interconnect between stacked packages". This application and all the said related applications are being filed on the same date, and each of the said related applications is hereby incorporated herein by reference.

BACKGROUND

[0003] This invention relates to semiconductor packaging.

[0004] Portable electronic products such as mobile phones, mobile computing, and various consumer products require higher semiconductor functionality and performance in a limited footprint and minimal thickness and weight at the lowest cost. This has driven the industry to increase integration on the individual semiconductor chips.

[0005] More recently the industry has begun implementing integration on the "z-axis," that is, by stacking chips, and stacks of up to five chips in one package have been used. This provides a dense chip structure having the footprint of a one-chip package, in the range of 5 x 5 mm to 40 x 40 mm, and obtaining thicknesses that have been continuously decreasing from 2.3 mm to 0.5 mm. The cost of a stacked die package is only incrementally higher than the cost of a single die package and the assembly yields are high enough to assure a competitive final cost as compared to packaging the die in individual packages.

[0006] The primary practical limitation to the number of chips that can be stacked in a stacked die package is the low final test yield of the stacked-die package. It is inevitable that some of the die in the package will be defective to some extent, and therefore the final